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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/273,560	03/22/99	HASEGAWA	T Q53743

EXAMINER

TM02/1012
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

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1- File Copy

Office Action Summary	Application No. 09/273,560	Applicant(s) HASEGAWA, TAKUMI	
	Examiner Kandasamy Thangavelu	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 1999 and 12 May 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3 and 4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Introduction

1. Claims 1 to 4 of the Application 09/273560 filed on 22 March 1999 are pending.

Foreign Priority

2. Acknowledgment is made of applicant's claim for foreign priority based on an application 10-100474 filed in Japan on March 27, 1998. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file. The papers have not been perfected.

Information Disclosure Statement

3. Acknowledgment is made of the information disclosure statements filed on March 22, 1999 and the notice of relevance filed on May 12, 2000. The notice of relevance has been considered in reviewing the claims.

Drawings

4 Figure 1 is objected to because the margin on the right side is too small. See MPEP § 608.02.

Specification

5 The disclosure is objected to because of the following informalities:

Page 6 Line 11 "the delay time of 2 ns" is inconsistent with line 15, "from low to high is 5 ns".

Page 6 Line 13 "(terminal1) is inconsistent with line 15, "from low to high is 5 ns".

Page 6 Line 15 "goes from low to high (falls)" is contradictory.

Appropriate corrections are required.

Claim Objections

6. The following is a quotation of 37 C.F.R § 1.75 (d)(1):

> The claim or claims must conform to the invention as set forth in the remainder of the specification and terms and phrases in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description.

7. Claim 3 is objected to because of the following informalities.

Page 12 Lines 14-15 "said at least of circuits" is grammatically incorrect.

Page 13 Lines 15-16 "said at least of circuits" is grammatically incorrect.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

This issue arises because Applicant refers to, Page 10, Lines 12-13, "delay analysis of the logic

circuit including at least one of the plurality of circuits" and Page 10, Lines 14-16, " A delay time between the input terminal and the output terminal is selected according to a logical operation of at least one of the circuits". It is to be understood that all delay analysis in the logic circuit will take into account logical operation of the individual circuit elements.

Claim Analysis, Interpretation and Prior Art

10. Claim 1 specifies:

1. Delay analysis system for delay analysis of a logic circuit.
2. A delay analysis library.
3. The library containing connection information on a plurality of circuits.
4. The library containing the delay time information on rises and falls of each input terminal and output terminal.
5. The library further contains logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal.
6. The delay time between the input terminal and the output terminal is selected according to a logical operation of one of the circuits.
7. The delay time between the input terminal and the output terminal is selected from the delay time information on the rises and falls of the input and the output terminals of the circuit.
8. The delay time information is stored in the library and delay calculations performed.

11. **Blinne et al.** (**BL**) (U.S. Patent 5,274,568) teaches that:

1. It deals with methods of estimating the delay times associated with integrated circuit cells (Col 1, Lines 7-9).
2. It deals with methods of emulating the delay times associated with individual cells such as those in ASIC arrays, including cell libraries (Col 1, Lines 9-13).
3. It deals with a process for designing and fabricating an integrated circuit using a cell library (Col 1, Lines 39-40). .
4. It comprises the step of emulating the delay time for the initial cell design ((Col 1, Lines 41-42).
5. It comprises the step of further developing the cell design and emulating the delay time for the developed cell (Col 1, Lines 42-45).
6. Each emulation step comprises determining the delay time of at least the rising edge or the falling edge of a signal through the cell (Col 1, Lines 45-48).

Lembach et al. (LM) (U.S. Patent 4,698,760) teaches that:

1. It deals with a method for optimization of signal timing delays (Col 1, Lines 9-10).
2. Such circuits function by detecting the presence or absence of signals at predetermined input terminals, performing various predesigned logical combinations on the basis of these detected signals and developing output signals for subsequent processing (Col 1, Lines 20-26).
3. One or more standardized cells are interconnected to form various logic combinations (Col 1, Lines 37-38).
4. This paper describes a delay calculator/optimizer program that calculates the circuit delay (Col 2, Line 35).

12. The correlation between Claim 1 and prior art is as follows:

1. The claim specifies "Delay analysis system for **delay analysis of a logic circuit**". **BL** specifies, Col 1, Lines 7-9, "It deals with methods of estimating the **delay times associated with integrated circuit** cells".
2. The claim specifies "A **delay analysis library**". **BL** specifies, Col 1, Lines 9-13, "It deals with methods of emulating the **delay times** associated with individual cells such as those in ASIC arrays, **including cell libraries".**
3. The claim specifies "The **library containing connection information on a plurality of circuits**". **BL** specifies, Col 1, Lines 39-40, "It deals with a process for **designing and fabricating an integrated circuit using a cell library**".
4. The claim specifies "The library containing the **delay time information on rises and falls of each input terminal and output terminal**". **BL** specifies, Col 1, Lines 45-48, "Each emulation step comprises determining **the delay time of at least the rising edge or the falling edge of a signal through the cell** (Col 1, Lines 45-48)".
5. The claim specifies "The library further contains **logical operation information** representing correspondence between a logical value of each input terminal and the logical value of the output terminal". **LM** specifies, Col 1, Lines 20-26, "Such circuits function by detecting the presence or absence of signals at predetermined input terminals, **performing various predesigned logical combinations** on the basis of these detected signals and developing output signals for subsequent processing".
6. The claim specifies, "The delay time between the input terminal and the output terminal is selected according to a **logical operation** of one of the circuits". **LM** specifies, Col 1, Lines 20-26, "Such circuits function by detecting the presence or absence of signals at predetermined input terminals, performing various **predesigned logical combinations** on the

basis of these detected signals and developing output signals for subsequent processing".

7. The claim specifies, "The delay time between the input terminal and the output terminal is selected from the **delay time information on the rises and falls of the input and the output terminals of the circuit**". **BL** specifies, Col 1, Lines 45-48, "Each emulation step comprises determining the **delay time of at least the rising edge or the falling edge of a signal** through the cell".
8. The claim specifies, "The **delay time information is stored in the library** and delay calculations performed". **BL** specifies, Col 1, Lines 9-13, "It deals with methods of emulating the delay times associated with individual cells such as those in ASIC arrays, including cell libraries".

13. Claim 3 specifies:

1. A method of making delay analysis of a logic circuit.
2. Referencing as library information a delay analysis library.
3. The library containing connection information on a plurality of circuits.
4. The library containing the delay time information on rises and falls of each input terminal and output terminal.
5. The library contains logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal.
6. Selecting the delay time between the input terminal and the output terminal as the delay time during rise or fall of the output terminal of circuit.
7. Selecting the delay time between the input terminal and the output terminal according to a logical operation of one of the circuits.
8. Selecting the delay time between the input terminal and the output terminal from the delay time information on the rises and falls of the input and the output terminals of the circuit.
9. The delay time information is stored in the library to perform delay calculations.

14. The correlation between Claim 3 and prior art is as follows:

1. The claim specifies "A **method** of making **delay analysis of a logic circuit**". **BL** specifies, Col 1, Lines 7-9, "It deals with methods of estimating the **delay times associated with integrated circuit** cells".
2. The claim specifies "Referencing as **library information** a delay analysis library". **BL** specifies, Col 1, Lines 9-13, "It deals with methods of emulating the **delay times** associated with individual cells such as those in ASIC arrays, including **cell libraries".**

3. The claim specifies "The **library containing connection information on a plurality of circuits**". **BL** specifies, Col 1, Lines 39-40, "It deals with a process for **designing and fabricating an integrated circuit using a cell library**".
4. The claim specifies "The library containing the **delay time information on rises and falls of each input terminal and output terminal**". **BL** specifies, Col 1, Lines 45-48, "Each emulation step comprises determining **the delay time of at least the rising edge or the falling edge of a signal through the cell** (Col 1, Lines 45-48)".
5. The claim specifies, "The library contains **logical operation information** representing correspondence between a logical value of each input terminal and the logical value of the output terminal". **LM** specifies, Col 1, Lines 20-26, "Such circuits function by detecting the presence or absence of signals at predetermined input terminals, **performing various predesigned logical combinations** on the basis of these detected signals and developing output signals for subsequent processing".
6. The claim specifies, "Selecting the delay time between the input terminal and the output terminal as the delay time during rise or fall of the output terminal of circuit". **LM** specifies, Col 1, Lines 20-26, "Such circuits function by detecting the presence or absence of signals at predetermined input terminals, performing various **predesigned logical combinations** on the basis of these detected signals and developing output signals for subsequent processing".
7. The claim specifies, "Selecting the delay time between the input terminal and the output terminal according to a **logical operation** of one of the circuits". **LM** specifies, Col 1, Lines 20-26, "Such circuits function by detecting the presence or absence of signals at predetermined input terminals, performing various **predesigned logical combinations** on the basis of these detected signals and developing output signals for subsequent processing".
8. The claim specifies, "Selecting the delay time between the input terminal and the output terminal from the **delay time information on the rises and falls of the input terminal and the output terminal of the circuit**". **BL** specifies, Col 1, Lines 45-48, "Each emulation step comprises determining the **delay time of at least the rising edge or the falling edge of a signal** through the cell".
9. The claim specifies, "The **delay time information being stored in the library** to perform delay calculations0". **BL** specifies, Col 1, Lines 9-13, "It deals with methods of emulating the delay times associated with individual cells such as those in ASIC arrays, including cell libraries".

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

16. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Blinne et al. (BL)** in view of **Lembach et al. (LM)**.

The following rejection is based on the interpretation of Paragraph 12 above.

As per Claim 1, **BL** recites the delay analysis system for delay analysis of a logic circuit (See Col 1, Lines 7-9) (Item 1, in Paragraph 12 above).

BL also teaches a delay analysis library (See Col 1, Lines 9-13) (Item 2, in Paragraph 12 above).

BL also teaches the library containing connection information on a plurality of circuits (Col 1, Lines 39-40) (Item 3, in Paragraph 12 above).

BL also teaches the library containing the delay time information on rises and falls of each input terminal and output terminal (Col 1, Lines 45-48) (Item 4, in Paragraph 12 above).

BL also teaches the delay time between the input terminal and the output terminal is selected from the delay time information on the rises and falls of the input and the output terminals of the circuit (Col 1, Lines 45-48) (Item 7, in Paragraph 12 above).

BL also teaches the delay time information is stored in the library and delay calculations performed (Col 1, Lines 9-13) (Item 8, in Paragraph 12 above).

BL does not teach the library further contains logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal. **BL** also does not explicitly teach the delay time between the input terminal and the output terminal is selected according to a logical operation of one of the circuits.

LM teaches that such circuits function by detecting the presence or absence of signals at predetermined input terminals, performing various predesigned logical combinations on the basis of these detected signals and developing output signals for subsequent processing (Col 1, Lines 20-26) (Item 5, in Paragraph 12 above).

It would have been obvious to one of ordinary skill in the art at the time of the invention that it was not necessary to store the logical information in the tables of the library, as the circuits automatically detected the signals and performed the logical operations on the basis of those signals developing output signals for subsequent processing. Therefore, the artisan would apply the teachings of **LM** to determine that it was not necessary to store the logical information in the tables of the library. The artisan would be motivated to not store the logical information in the tables of the library as the information was inherent in the digital circuits and hence was redundant. He would also be motivated to avoid wastage of memory space and computer time.

It would also have been obvious to one of ordinary skill in the art at the time of the invention that the delay time between the input terminal and the output terminal need not be selected according to a logical operation of one of the circuits as the delay times computed by **BL** had taken into account the logical operations involved. So the logical operation need not be used as a selection factor. The artisan would have been motivated to not use the logical

operation involved, as it had already been taken into account by the method of **BL** and the artisan would prefer to simplify the selection process.

17. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Blinne et al. (BL)** in view of **Lembach et al. (LM)**. Claim 2 is a duplicate of Claim 1 except for minor differences.

The following rejection is based on the interpretation of Paragraph 12 above.

As per Claim 1, **BL** recites the delay analysis system for delay analysis of a logic circuit (See Col 1, Lines 7-9) (Item 1, in Paragraph 12 above).

BL also teaches a delay analysis library (See Col 1, Lines 9-13) (Item 2, in Paragraph 12 above).

BL also teaches the library containing connection information on a plurality of circuits (Col 1, Lines 39-40) (Item 3, in Paragraph 12 above).

BL also teaches the library containing the delay time information on rises and falls of each input terminal and output terminal (Col 1, Lines 45-48) (Item 4, in Paragraph 12 above).

BL also teaches the delay time between the input terminal and the output terminal is selected from the delay time information on the rises and falls of the input and the output terminals of the circuit (Col 1, Lines 45-48) (Item 7, in Paragraph 12 above).

BL also teaches the delay time information is stored in the library and delay calculations performed (Col 1, Lines 9-13) (Item 8, in Paragraph 12 above).

BL does not teach the library further containing logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal. **BL** also does not explicitly teach the delay time between the input terminal and the output terminal is selected according to a logical operation of circuits.

LM teaches that such circuits function by detecting the presence or absence of signals at predetermined input terminals, performing various predesigned logical combinations on the basis of these detected signals and developing output signals for subsequent processing (Col 1, Lines 20-26) (Item 5, in Paragraph 12 above).

It would have been obvious to one of ordinary skill in the art at the time of the invention that it was not necessary to store the logical information in the tables of the library, as the circuits automatically detected the signals and performed the logical operations on the basis of those signals developing output signals for subsequent processing. Therefore, the artisan would apply the teachings of **LM** to determine that it was not necessary to store the logical information in the tables of the library. The artisan would be motivated to not store the logical information in the tables of the library, as the information was inherent in the digital circuits and hence redundant. He would also be motivated to avoid wastage of memory space and computer time.

It would also have been obvious to one of ordinary skill in the art at the time of the invention that the delay time between the input terminal and the output terminal need not be selected according to a logical operation of circuits as the delay times computed by **BL** had taken into account the logical operations involved. So the logical operation need not be used as a selection factor. The artisan would have been motivated to not use the logical operation involved, as it had already been taken into account by the method of **BL** and the artisan would prefer to simplify the selection process.

18. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Blinne et al. (BL)** in view of **Lembach et al. (LM)**.

The following rejection is based on the interpretation of Paragraph 14 above.

As per Claim 1, **BL** recites a method for making a delay analysis of a logic circuit (See Col 1, Lines 7-9) (Item 1, in Paragraph 14 above).

BL also teaches referencing as library information a delay analysis library (See Col 1, Lines 9-13) (Item 2, in Paragraph 14 above).

BL also teaches the library containing connection information on a plurality of circuits (Col 1, Lines 39-40) (Item 3, in Paragraph 14 above).

BL also teaches the library containing the delay time information on rises and falls of each input terminal and output terminal (Col 1, Lines 45-48) (Item 4, in Paragraph 14 above).

BL also teaches selecting the delay time between the input terminal and the output terminal as the delay time during rise and fall of the output terminal of the circuit (Col 1, Lines 45-48) (Item 6, in Paragraph 14 above).

BL also teaches selecting the delay time between the input terminal and the output terminal from the delay time information on the rises and falls of the input and the output terminals of the circuit (Col 1, Lines 45-48) (Item 8, in Paragraph 14 above).

BL also teaches the delay time information being stored in the library to perform delay calculations (Col 1, Lines 9-13) (Item 9, in Paragraph 14 above).

BL does not teach the library containing logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal. **BL** also does not explicitly teach selecting the delay time between the input terminal and the output terminal according to a logical operation of one of the circuits.

LM teaches that such circuits function by detecting the presence or absence of signals at predetermined input terminals, performing various predesigned logical combinations on the basis

of these detected signals and developing output signals for subsequent processing (Col 1, Lines 20-26) (Item 5, in Paragraph 14 above and Item 7, in Paragraph 14 above).

It would have been obvious to one of ordinary skill in the art at the time of the invention that it was not necessary to store the logical information in the tables of the library, as the circuits automatically detected the signals and performed the logical operations on the basis of those signals developing output signals for subsequent processing. Therefore, the artisan would apply the teachings of **LM** to determine that it was not necessary to store the logical information in the tables of the library. The artisan would be motivated to not store the logical information in the tables of the library as the information was inherent in the digital circuits and hence was redundant. He would also be motivated to avoid wastage of memory space and computer time.

It would also have been obvious to one of ordinary skill in the art at the time of the invention that the delay time between the input terminal and the output terminal need not be selected according to a logical operation of one of the circuits as the delay times computed by **BL** had taken into account the logical operations involved. So the logical operation need not be used as a selection factor. The artisan would have been motivated to not use the logical operation involved, as it had already been taken into account by the method of **BL** and the artisan would prefer to simplify the selection process.

19. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Blinne et al. (BL)** and **Lembach et al. (LM)** in view of **Jun et al (JN)**.

The following rejection is based on the interpretation of Paragraph 14 above.

As per Claim 4, **BL** and **LM** teach the methodology of the claim as discussed in regards to Claim 3 above. **BL** and **LM** also teach the step of performing the delay calculation with selected delay time as propagation delay time of the circuit (Item 1, Paragraph 14 above).

BL and **LM** do not teach a computer readable medium having stored thereon a program for executing the process for delay analysis using the method of Claim 4.

JN teaches that with the progress of semiconductor technology, software simulation has become indispensable for design verification (Page 2117, Col 1, Para2). In the simulation of digital circuits accurate calculation of rise/fall delay times is most important, which can be done by circuit or timing simulators (Page 2117, Col 1, Para2).

It would have been obvious to one of ordinary skill in the art at the time of the invention to determine that the BL and LM method for developing the delay times for the logic circuits need to be implemented on a proper computer using a programming language so it can be repetitively used with different logic circuits. The simulation program would have been developed. The program would use the existing library of the delay times and would add to the library as more simulations were performed. Having developed the simulation program, the artisan would have used it to develop the delay times for various circuits. The program would have been implemented on a computer readable medium.

The artisan would have used **JN**'s method of developing the simulations as it would have facilitated analysis of many circuits in minimal time.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kandasamy Thangavelu whose telephone number is

703-305-0043. The examiner can normally be reached on Monday through Friday from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
October 1, 2001

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER